Keep-Out-Zone Analysis for Three-Dimensional ICs

Names are hidden due to the blind review required

***Abstract*—Three-dimensional (3D) integration using through-silicon vias (TSVs) offers many advantages over traditional 2D integration, however there are still several challenges originated from stacking dies. One of main challenges of 3D-integration is the area overhead which has two main causes: first the huge TSV diameter which is usually in the range of microns, and the second reason is the keep-Out-Zone (KOZ) overhead due to the high induced thermal stresses during fabrication. The area overhead besides the fabrication process itself inversely affect the overall yield and cost, so the increase in area will reduce the yield and increase the cost. In this paper, the effect of KOZ overhead on the overall area, yield, and cost is investigated. Also various parameters that might change KOZ overhead are examined. In this paper, we show that the share of area overhead caused by KOZ is pretty higher compared to that of TSVs. Further, the impact of KOZ is considered for obtaining more accurate estimation on W2W overall yield and cost of a 3D-IC.**

I. Introduction

In recent years, with the huge advancement in IC fabrication technology, transistor dimensions keep shrinking leading to have more and more modules on the same chip. However, such shrinking creates a lot of challenges to traditional ICs (2D-ICs) to keep following Moore's law. It is because the increase in the average wire length results in larger area, as well as higher delay and power consumption. Another problem is the increase in clock delay within the chip which leads to the lack of synchronization [1].

TSV-based 3D integration has been proposed as a promising solution to overcome the above mentioned issues of conventional 2D integration. 3D integration introduces several advantages such as shorter interconnections, lower signal delay, higher degree of integration density, and lower mask cost. However TSVs pose multiple challenges as well. One important challenge is the large area overhead caused by the TSV and Keep-Out-Zone [2]. The importance of area overhead problem is that it affects inversely the overall yield and cost of the 3D chip. Therefore reducing the area overhead could enhance the most important fabrication and reliability parameters of the chip; area, yield, and cost.

Some recent techniques reduce area overhead by reducing TSV count by multiplexing [3], serialization [4] or virtualization [5], to mitigate the side effects of the TSVs. Although, the advantages of reducing TSV count on area is discussed in [3]-[5], its influence on KOZ overhead has not been studied yet. We expect that KOZ is most likely affected by reducing TSV count due to a probable change in stress distribution across die.

While the analysis in [3] considers that KOZ is independent of TSV count, in this paper, we reintroduce the TSV-BOX concept discussed in [3], but with more detailed analysis regarding the effect of the reduced number of TSVs on KOZ. TSV-BOX reduces the footprint area of TSVs, thus as a direct impact it improves the fabrication yield and reduces the fabrication cost as well. Using a simple 2×1 Multiplexer (MUX) in one layer (die) and a 1×2 demultiplexer (DeMUX) in the other layer of the 3D stack, the two digital signals can be transferred over one TSV instead of two, hence leading to 50% reduction in total TSV count.

In the rest of this paper, section 2 is a background section detailing TSV-BOX technique and KOZ concept. Section 3 highlights sample model used in KOZ analyses. The experimental results are discussed and described as well in this section. Finally, Section 4 concludes the paper.

II. Background

A. The TSV-BOX

As shown in Fig. 1(a). The two input digital signals to be multiplexed are (V_1, V_2) while ($V_1^{'}$, $V_2^{'}$) are the two outputs which represent (V_1, V_2), respectively. As shown in Fig. 1(b) both the MUX and the DeMUX are implemented using two transmission gates. The SEL signal (Fig. 1(c)) is used for input selection. It is chosen to have low aspect ratio (here it is 1/10) for the sake of smaller power overhead of the TSV-BOX, and to preserve the sameness between input and output signals [3]. In addition to that, T_H+T_L must be equal to duration of one clock period. Depending on the value of the selection signal (SEL) one of two inputs to the TSV-BOX namely, V_1 or V_2 passes through the TSV. Consequently, $V_1^{'}$ and $V_2^{'}$ at the output of the DeMUX represent V_1 and V_2, respectively. According to the operation of the TSV-BOX (Fig. 2), it is observable that $V_2^{'}$ is exactly equal to V_2 and $V_1^{'}$ is a delayed version of V_1. The delay is very small equal to the period of the high pulse T_H of the SEL signal. Since T_H is very small we can say that $V_1^{'} \approx V_1$. The complete proof for TSV-BOX and the timing requirements for all signals is found in [3].

B. Keep-Out-Zone

During the bonding process of 3D-IC fabrication, the bonding temperature can reach 300°C [6]. Such high temperature difference induces thermal stresses in the area nearby TSVs due to the mismatch between the coefficient of thermal expansion (CTE) of copper TSVs and the surrounding substrate silicon. Due to the piezoresistivity property of silicon, the induced thermal stresses change the mobility of the carriers of the silicon nearby the TSVs. Such change in mobility can result in timing violations in the implemented circuit.

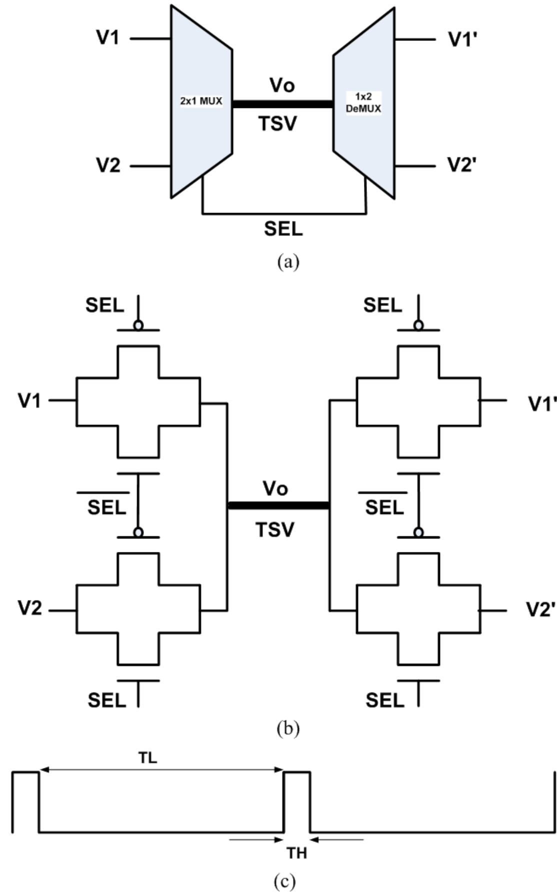

Fig. 1: (a) TSV-BOX schematic, (b) TSV-BOX circuit implementation, (c) Selection signal (SEL).

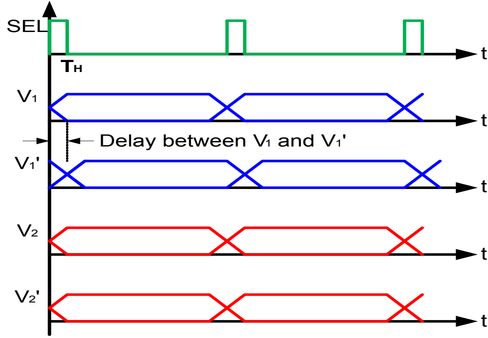

Fig. 2: SEL(t), V_1(t), $V_1{}'$(t), V_2(t), and $V_2{}'$(t).

Therefore a keep-Out-Zone area is proposed so that it is forbidden to implement any circuit in this area (Fig. 3). Usually the KOZ is considered the area around TSV in which the change in mobility is more than 5% [7]. The change in mobility depends on different parameters and constants: the first one is the transistor channel orientation around TSV. The well known channel alignments are [100] and [110] where in the first one the channel is aligned horizontally in the X direction and in the second one the channel is a aligned with 45° angle to X direction (Fig. 4). The second parameter is the piezoresistivity coefficients of silicon which in turn dependant on the carrier mobility type and its concentration in silicon [8]. Finally, the most important parameter for this study is the normal stress induced nearby the TSVs due to temperature change. According to [7], the percentage change in mobility along [100] channel direction is:

$$\frac{\Delta\mu}{\mu}|_{[100]} = |\pi_{11}\sigma_1 + \pi_{12}(\sigma_2 + \sigma_3)| \tag{1}$$

where σ_1, σ_2, and σ_3 are the X, Y, and Z components of the normal stress, while π_{11} and π_{12} are the piezoresistivity coefficients of silicon. If the channel direction is in [110] then a transformation is required for all coefficients and parameters in Eq. 1. Then the mobility change in [110] direction will be [7]:

$$\frac{\Delta\mu}{\mu}|_{[110]} = |\frac{\pi_{11} + \pi_{12}}{2}(\sigma_1 + \sigma_2) + \pi_{44}\sigma_{12}| \tag{2}$$

where π_{44} is another coefficient in the piezoresistivity matrix of silicon.

III. 3D-IC sample model and Experimental Result

A. The 3D-IC KOZ model investigated

The model used to investigate the 3D-IC thermal stress behaviour is shown in Fig. 5. Because of the symmetry in TSV distribution only a repeated square structure of sixteen TSVs (or eight TSVs in case TSV-BOX is used) will be considered and used for simulations. Fig. 5(b) shows the same model but for the TSV-BOX with just eight TSVs. The dimensions of the square structure is as follows, the length is four TSV pitches ($4P$) and the thickness is assumed constant at 20μm. The mechanical properties assumed for silicon and copper used are stated in Table I and Table II [7]. The model is tested under temperature difference ΔT=300°C which is the bonding temperature explained in section 2-B.

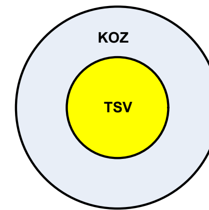

Fig. 3: Keep-Out-Zone (KOZ) around TSV.

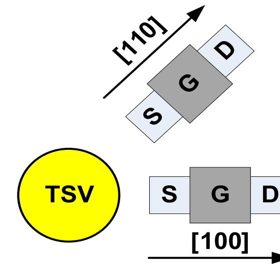

Fig. 4: Transistor channel orientations around the TSV.

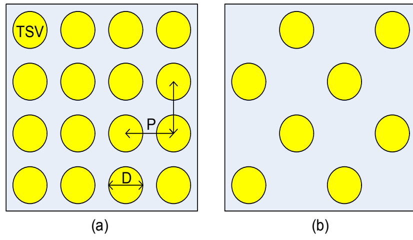

Fig. 5: 3D-IC sample model (a) without TSV multiplexing, (b) TSV-BOX case with reduced TSV count.

TABLE I: Material properties of the implemented model

Material	Youngs Modulus (GPa)	Poisson Ratio	CTE (ppm/°C)
Si	169	0.26	2.3
Cu	117	0.3	16.7

TABLE II: Piezoresistivity coefficients for silicon (in units of 10^{-11} Pa^{-1})

Doping type	π_{11}	π_{12}	π_{44}
n-type Si	-102.2	53.7	-13.6
p-type Si	6.6	-1.1	138.1

B. Experimental Results

In this section various experiments are conducted to investigate the impact of KOZ on 3D-ICs area overhead. All the experiments shown in this section are performed for [100] channel orientation. Although the same experiments are done for [110] orientation and the same conclusions have been derived but they are not shown in this paper due to the lack of space.

1) The effect of bonding and operating temperatures: 3D-ICs are exposed to different temperature differences during fabrication and normal 3D-IC operation. In this experiment the effect of different temperature differences on KOZ is investigated. The bonding temperature difference is ΔT=300°C as stated before, while the normal operation temperature difference is assumed to be ΔT=75°C (variation between 25°C and 100°C). Fig. 6 shows the KOZ area overhead for the two above cases. As expected, the higher temperature difference, the more increase in KOZ. The same behaviour also occurs when TSV count reduces via using TSV-BOX. In this case, the bonding temperature which is very high compared to the operating temperature results in very large KOZ for all Pitch/Diameter (*P/D*) ratios tested. Consequently, referring to results whown in Fig. 6, only the bonding temperature should be considered for KOZ measurements.

2) The area overhead of KOZ: The TSV-BOX introduced in [3], reduces the TSV count by 50%. However, the area analyses conducted in [3] do not consider the effect of TSV count alteration on KOZ variation. Fig. 7, shows the area overhead of KOZ and TSVs before and after TSV multiplexing using TSV-BOX for n-type transistor channels. As shown, the KOZ overhead is the largest component of the overhead. Also, it is observed that, although the TSV-BOX has reduced the TSV overhead by 50%, the reduction in TSV count has very small effect on KOZ for small *P/D* ratio. For high *P/D* ratios the situation seems better, where the reduction in KOZ overhead is almost the same as TSV overhead, i.e. as the TSV count reduces by 50%, KOZ area overhead reduces by about 50% as well. Fig. 8 verifies the previous notes on KOZ overhead, where it is clear that the KOZ overhead becomes about 50% after *P/D*=3. For p-type channels oriented in [100] direction, the situation is slightly different. The KOZ overhead is comparable to the TSV overhead. However, the KOZ overhead is still large reaching about 40% of the total overhead especially for small *P/D*.

3) The effect of KOZ on the percentage area reduction of TSV-BOX: According to the previous discussion, the main advantage of the TSV-BOX which is reducing the overhead area by 50% is not completely gained, especially in n-type [100] case (Fig. 9). This is because the behaviour of KOZ variation in relation to the reduction of TSV count is dependent on *P/D* ratio. Therefore the 50% area reduction will be gained only for high *P/D* ratios at which the KOZ reduction reaches 50% as well. For p-type [100] case, the situation is better, as the reduction of KOZ overhead with TSV count is always

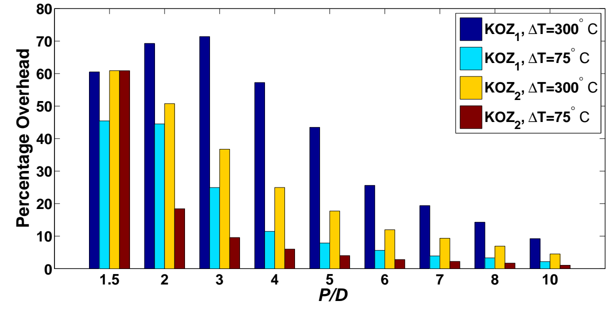

Fig. 6: Bonding and operating temperature effect on KOZ for various *P/D* ratios (KOZ_1 and KOZ_2 are the KOZ before and after TSV multiplexing).

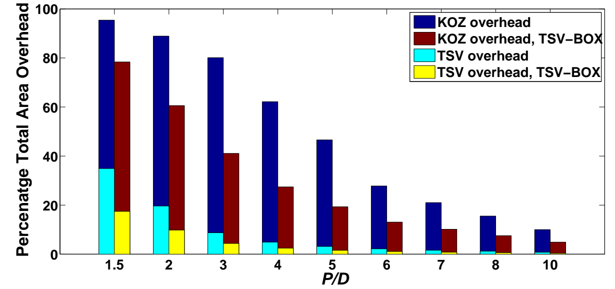

Fig. 7: Area overhead components before and after TSV multiplexing.

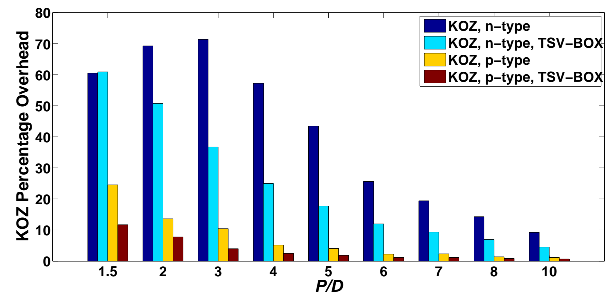

Fig. 8: KOZ overhead comparison before and after TSV multiplexing.

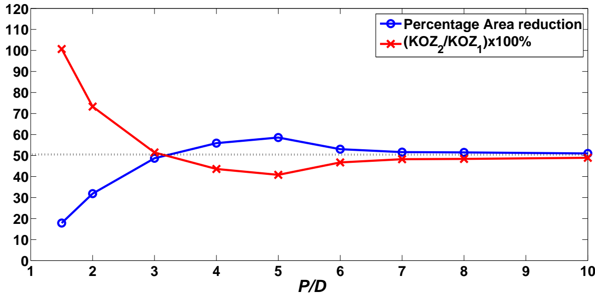

Fig. 9: Percentage area reduction and KOZ variation versus *P/D* for n-type carriers.

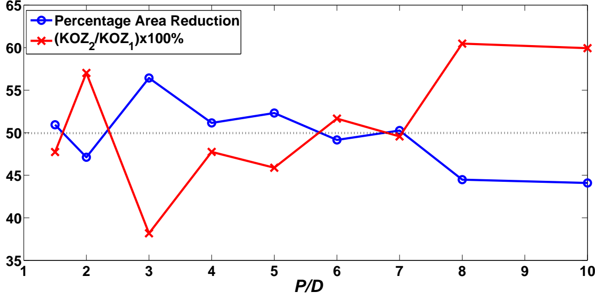

Fig. 10: Percentage area reduction and KOZ variation versus *P/D* for p-type carriers.

around 50% for small and high *P/D*, as shown in Fig. 10.

4) Yield enhancement of the TSV-BOX: Using the previous calculations of the KOZ variation in response to the variation of TSV count, more accurate calculations on the overall W2W yield and cost than the ones stated in [3] can be done. The analysis is similar to the one in [3] but with additional consideration of KOZ variation with respect to the TSV count. Fig. 11 shows the variation of the W2W overall normalized yield ($Y_{W2W-norm}$) in response to the variation of TSV count under different *P/D* ratio and constant die area of 100 mm^2. As expected the larger the TSV count, the larger will be the normalized yield. This is because for a large TSV count the overhead caused by TSVs and KOZ will be large as well compared to die area. This obviously results in a more clear reduction in area using TSV-BOX, hence the enhancement in yield gained will be higher as well, which exceeds 10000 times the original W2W yield for the 3D-IC without TSV-BOX. The effect of KOZ on the overall yield can be observed as well. As shown in Fig. 11, the highest peak always appears for *P/D*= 5. Since at such point, the percentage reduction in area is the most due to the minimum KOZ (Fig. 9).

5) Cost reduction: In this subsection, the normalized overall cost is estimated according to Dong model in [9]. According to [3], the normalized overall W2W cost ($C_{W2W-norm}$) can calculated as:

$$C_{W2W_{norm}} = \frac{1}{Y_{W2W_{norm}}} \quad (3)$$

Fig. 12 shows the cost reduction for the TSV-BOX versus TSV count. The result of analysis on the cost is similar to what described for the overall yield.

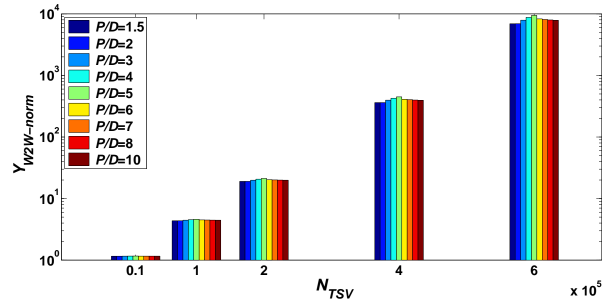

Fig. 11: W2W normalized yield versus TSV count.

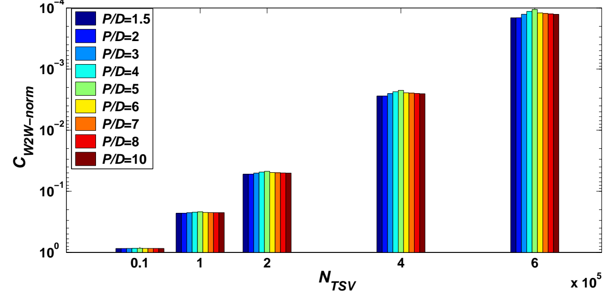

Fig. 12: W2W normalized cost versus TSV count.

IV. Conclusion and Future Work

In this paper, an intensive Keep-Out-Zone experimental investigation was introduced. The effect of bonding as well as operating temperatures of 3D-ICs on KOZ were tested. It is found that the bonding temperature results in large KOZ, therefore only the bonding temperature should be considered for KOZ measurements. Also, the effect of TSV count on KOZ was investigated. It is observed that, for large *P/D* ratios, TSV multiplexing techniques such as TSV-BOX can reduce the KOZ as well as TSV area overhead only for large *P/D*, otherwise the reduction in KOZ is almost negligible.

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