Design Methodology Deduction for 3D Network-on-Chip with Multiplexed Through-Silicon Vias

ABSTRACT

3D integration is an emerging technology that overcomes 2D integration process limitations. The use of short Through-Silicon Vias (TSVs) introduces a significant reduction in routing area, power consumption, and delay. Though, there are still several challenges in 3D integration technology need to be addressed. It is shown in literature that reducing TSV count has a considerable effect in improving yield. The TSV multiplexing technique called TSVBOX was introduced in [1] to reduce the TSV count without affecting the direct benefits of TSVs. The TSVBOX introduces some delay to the signals to be multiplexed. In this paper, we analyse the TSVBOX timing requirements and deduce a design methodology for TSVBOX-based 3D Network-on-Chip (NoC) to overcome the TSVBOX delay degradation. Performance comparisons under different traffic patterns are conducted to verify our solution. We show that TSVBOX-based 3D NoC performance is highly dependent on the NoC traffic pattern and in most simulation scenarios we tried, it shows almost the same performance of the conventional 3D NoC.

Keywords

Network-on-Chip (NoC), Yield, Through-Silicon Vias (TSVs)

1. INTRODUCTION

2D integration proves to have many limitations for nowadays large systems needs. On the other side, 3D integration is an emerging technology that can mitigate these significant issues. However there are still some challenges that need more and more focus to make such promising technology mature and reliable. One of these challenges is the reliability issue in terms of yield. 3D-ICs show very low yield due to extra fabrication steps of bonding dies or wafers to each other to create the 3D stack. These extra steps may result in some faulty TSVs [2]. The probability of having faulty TSVs increases as the total number of TSVs increases. Hence, finding a technique that reduces TSV count without affecting the benefits gained by 3D integration is crucial. The TSV multiplexing technique introduced in [1] reduces the number of TSVs by half, by multiplexing each two 3D signals[1] into one signal and passing this signal through one TSV instead of two. Therefore almost 50% reduction in TSV count is achieved. Due to this significant reduction in TSV count, the analysis done in [1] on yield has revealed very high improvement over conventional 3D-ICs. The TSVBOX uses extra selection signal (SEL) to control a multiplexer/demultiplexer assembly. This SEL signal introduces some delay to one of the multiplexed signals besides the parasitics of the TSVBOX itself. Such delay may affect the functional validity of the system to be implemented using TSVBOX. Although, [1] addresses most of the issues related to TSVs multiplexing, such delay problem has not been studied yet.

Due to its scalability and novelty as a multicore communication architecture for future multiprocessor SoCs, 3D NoC is selected as our target system architecture for applying the TSVBOX technique. Using this architecture, timing requirements and the design methodology for TSVBOX-based 3D NoC are investigated so that the performance degradation is avoided.

The rest of this paper is organized as follows: Section 2 introduces TSVBOX technique. Section 3 explores the target 3D NoC architecture. Section 4 highlights the TSVBOX circuit model and various design aspects. Section 5 introduces the TSVBOX timing analyses and our design methodology that tackles delay degradation of the TSVBOX. The simulation results are discussed and justified in Section 6. Finally, Section 7 concludes the paper.

2. TSVBOX

As shown in Fig. 1a, the TSVBOX is composed of a multiplexer (MUX), a demultiplexer (DeMUX), and a TSV in between. The selection signal (SEL), shown in Fig. 1b, is used to control the circuit. Referring to [1], using the TSVBOX circuit, V_1 and V_2 signals can be transferred over one TSV instead of two as in the conventional 3D-ICs. Ideally, V_2 will pass with no delay, thus $V_2{}'$=V_2, and V_1 will be delayed by T_H so $V_1{}'(t)$=$V_1(t - T_H)$. Therefore T_H should be selected such that; $T_H \ll T_{CLK}$ in general. The proof of this concept and more detailed analysis are in [1].

3. THE TARGET 3D NOC ARCHITECTURE

Fig. 2 shows our target 3×3×2 mesh topology 3D NoC architecture. The packet size *N* is assumed to be equivalent to the data bus width. For the conventional 3D NoC, the whole 3D data bus width is $N+2$, where the extra two bits are required for the synchronous handshaking protocol which needs request (*REQ*) and acknowledgement (*ACK*) signals. For the TSVBOX case, the data bits of the packet are multiplexed and hence $\frac{N}{2}+2$ TSVs are required. However for each vertical bus width two extra TSVs are required to transfer the SEL signal and its inverted version $\overline{SEL}$. Therefore,

[1]A 3D signal is the signal that traverses from one layer to another in the 3D stack.

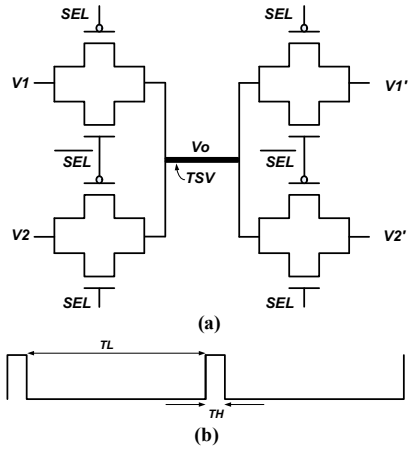

Figure 1: (a) TSVBOX circuit, (b) SEL selection signal.

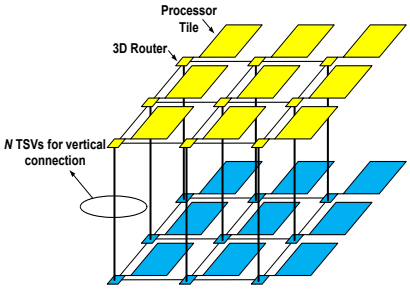

Figure 2: The 3×3×2 3D NoC architecture.

the vertical connection bus width is $\frac{N}{2}+4$ for the TSVBOX-based 3D NoC. For simplicity, Store-And-Forward and XYZ deterministic routing are chosen to be the 3D NoC switching technique and routing algorithm, respectively. Each port has one FIFO buffer of five packets size, where the packet size is 32 bits. Each router is connected through the local port to a processor core which is modeled as a random packet generator/consumer for the router.

4. DESIGN CONSIDERATIONS AND MODELING

Since Spice models for such system would be too complicated and time consuming either in design or simulation, SystemC-A is used for our 3D NoC implementation. Processor cores, routers, and intra-layer interconnects, are modeled as a high level architectures, while for inter-layer interconnects (the vertical connections); TSVs and TSVBOX, low level circuit implementation is used to be able to accurately determine different delays. Different design considerations are listed as follows:

- 3D path model: As shown in Fig. 3a, the 3D signal is assumed to pass through an input inverter driver, a global wiring segment in the first layer, a TSV, a global wiring segment in the second layer, and an output inverter driver. The output inverter driver is assumed always 1x-inverter (minimum size inverter).
- TSV and wiring parasitics: For the TSV and wiring circuit models, the models introduced in [4, 5] are used (Fig. 3d and 3e, respectively). According to [6], C_{TSV} and R_{TSV} can be assumed to be 15 fF and 1Ω, respectively. Wiring is assumed to be global. The length of the global wires is assumed 200 μm [6]. Global wiring parasitics are stated in Table 1 [7].
- Transistor model: The circuit models for both nMOS and pMOS are shown in Fig. 3d and 3e, respectively. The model parasitics and technology parameters are depicted in Table 1, based on 180 nm TSMC transistor model from TSMC [3].

Table 1: Transistor parasitics and technology parameters for TSMC 180 nm.

Transistor parasitic or technology parameter	Unit	TSMC 180 nm
C_{gP}	fF	2.06
C_{gN}	fF	2.06
C_{sbP}	fF	0.3348
C_{sbN}	fF	0.2016
C_{dbP}	fF	0.3348
C_{dbN}	fF	0.2016
R_{onP}	kΩ	24.111
R_{onN}	kΩ	14.944
C_W	fF/μm	0.269
R_W	Ω/μm	0.0363
$\|V_{thP}\|$	V	0.51
V_{thN}	V	0.53
V_{DD}	V	1.8

- Transmission gate transistors design: The TSVBOX is composed of four transmission gates, and according to [8], transmission gate transistors are usually selected to be minimum sized (K_N=K_P=*1*, where K_P *and* K_N are the sizes of pMOS and nMOS, respectively). Thus both nMOS and pMOS of the transmission gate will be selected such that; W_P=L_P=W_N=L_N, where W_P,W_N and L_P,L_N are the widths and lengths of pMOS and nMOS, respectively.
- Load capacitance: Since inverter driver load is assumed 1x-inverter, the input capacitance can be expressed as:

$$C_L = C_{gn} + 1.5 \times C_{gp} \quad (1)$$

where W_P=1.5L_P for pMOS to ensure equal currents during charging and discharging phases.

- *ON-OFF* threshold voltages of inverter drivers: There are two input thresholds: $V_{inL-max}$ which is the maximum low input voltage required to switch pMOS *ON* and nMOS *OFF* at the same time. Therefore if $V_{in} \leq V_{inL-max}$, nMOS will be *OFF* and pMOS will be *ON*. The other threshold voltage is $V_{inH-min}$, which is the minimum high input voltage required to switch nMOS *ON* and pMOS *OFF* at the same time, therefore if $V_{in} \geq V_{inH-min}$, nMOS will be *ON* and pMOS will be *OFF*. Referring to [3], for digital circuits, $V_{inL-max}$ and $V_{inH-min}$ can be calculated as follows:

$$V_{inL-max} = V_{thN}, V_{inH-min} = V_{DD} - |V_{thP}| \quad (2)$$

where $|V_{thP}|$, V_{thN}, and V_{DD} are shown in Table 1.

- *ON-OFF* threshold voltages of transmission gate switches: nMOS switches *ON* when $V_{gN} \geq V_{thnN}$, while for pMOS when $|V_{gP}| \geq |V_{thP}|$, therefore max(V_{thnN}, $|V_{thP}|$) is enough to meet both conditions. Following the same analysis, the *OFF* condition is min(V_{thnN}, $|V_{thP}|$). Since $V_{thnN} \approx |V_{thP}|$ in most technologies, so for simplicity we can assume that max(V_{thnN}, $|V_{thP}|$)≈min(V_{thnN}, $|V_{thP}|$)

4.1 Conventional 3D signal path modeling

The conventional 3D-IC 3D signal path is shown in Fig. 4 where the signal is assumed to pass through an inverter driver (represented by its *ON* resistance $R_{dr-Conv}$), the global wiring of the first layer, the TSV, the global wiring of the second layer, and the load capacitance which is the input gate capacitance of a 1x-inverter driver in

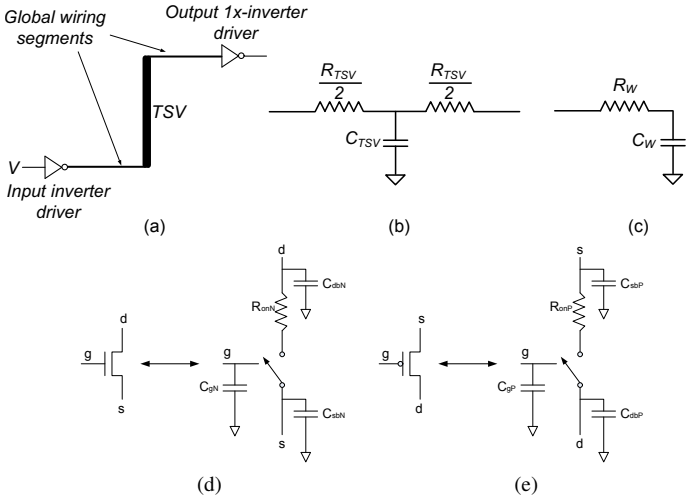

Figure 3: (a) The 3D signal path and circuit models of (b) TSV, (c) global wiring, (d) nMOS, and (e) pMOS.

the second layer. The conventional 3D NoC 3D signal path delay (T_{d-Conv}) can be approximated using Elmore-delay as follows:

$$T_{d-Conv} = \ln \frac{V_{DD}}{|V_{thP}|} \cdot \Big[R_{dr-Conv} \cdot (2C_W + C_{TSV} + C_L)\Big] \quad (3)$$

where the wiring and TSV resistances are neglected to simplify the analysis due to their very small values.

4.2 TSVBOX 3D signal path modeling

Fig. 5 shows the TSVBOX circuit model. It is similar to the circuit of the conventional 3D signal path, the difference is that the equivalent RC parasitic circuit of the transistors in MUX and DeMUX are involved. Since there is no transistor models in SystemC-A, the transistors of the transmission gate are modeled using perfect switches. The SEL signal controls the upper transmission gates of the MUX and the DeMUX, and its inverted version $\overline{SEL}$ controls the lower ones. Therefore both the lower and upper transmission gates will switch *ON* or *OFF* exclusively as required in the original TSVBOX design. The SEL signal path shown in Fig. 5, is similar to the conventional 3D signal path. However, the SEL signal is driving the gates of the transmission gates, therefore for each SEL path, there are four gate capacitances ($4C_g$) involved in the load; $2C_g$ from MUX and $2C_g$ from DeMUX. Then for $\frac{N}{2}$ data bus width, the TSVBOXes will contribute with $N \cdot (C_{gN} + C_{gP})$ in total to the SEL signal load.

The Elmore-delay for both V_1 and V_2 can be approximated according to the following equation:

$$\begin{aligned} T_{d-TSVBOX} = \ln \frac{V_{DD}}{|V_{thP}|} \cdot \Big[& R_{dr-TSVBOX} \cdot C_{PN} + \\ & (R_{dr-TSVBOX} + R_{PN}) \cdot (4C_{PN} + 2C_W + C_{TSV}) + \\ & (R_{dr-TSVBOX} + 2R_{PN}) \cdot (C_{PN} + C_L)\Big] \end{aligned} \quad (4)$$

where

$$C_{PN} = C_{dbP} + C_{dbN},\ R_{PN} = \frac{R_{onP} \cdot R_{onN}}{R_{onP} + R_{onN}}$$

While the delay of the SEL signal can be approximated by:

$$\begin{aligned} T_{d-SEL} = \ln \frac{V_{DD}}{V_{DD} - max(V_{thN},\ |V_{thP}|)} \cdot \\ \Big[R_{dr-SEL} \cdot (2C_W + C_{TSV} + 2N \cdot C_g)\Big] \end{aligned} \quad (5)$$

5. TIMING REQUIREMENTS ANALYSIS

5.1 Synchronous communication protocol

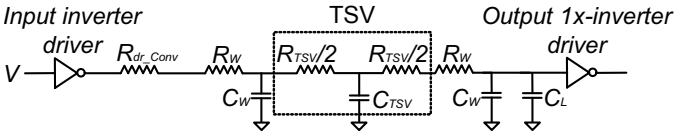

Figure 4: Conventional 3D NoC 3D path circuit model.

Fig. 6 shows the synchronous handshaking protocol between two routers which can be explained as follows:

(1) The transmitting router initiates a request to the receiving router by setting the *REQ* signal to '1'. At the same time it puts the data packet (*PKT*) on the data bus.

(2) After at least one cycle, the initiated request will be recognized by the input controller of the receiving router. If there is at least one free slot in the FIFO buffer, the packet will be read and the acknowledgement *ACK* signal will be set to '1', announcing the successful reception of the packet.

(3) Upon detecting the *ACK* signal, after one cycle, the transmitting router will reset the *REQ* to '0'. Resetting *REQ* is the end of the communication procedure.

According to this procedure, the packet must be ready at least one clock cycle after initiating the request. Therefore, the SEL signal can be chosen to be the clock signal itself. If so, in the first half of the clock cycle V_1 (V_2) will be transmitted, and vice versa in the second half cycle. As a result to this, it can be concluded that T_H=T_L=$\frac{1}{2}T_{CLK}$.

5.2 Power gating to *SEL* signal

It is observable from Fig. 6, that the SEL signal is only needed during packet transfer operation. To decrease the overhead in power consumption originated from the SEL signal, the power gating technique is applied to it using the *REQ* signal, as shown in Fig. 7. This transmission gate introduces some extra delay to the SEL path. In order to reduce this delay, the transmission gate is positioned before the input inverter driver of the SEL signal. For further reduction in delay, a 1x-inverter driver is introduced between the power gating transmission gate and the main inverter driver of the SEL signal. Therefore only the input capacitance of the 1x-inverter driver is considered in calculating the delay. This extra delay can be approximated as:

$$T_{d-PG} = \ln \frac{V_{DD}}{|V_{thP}|} \cdot [R_{PN} \cdot (C_{PN} + (K_N + K_P) \cdot C_g)] \quad (6)$$

where K_N=*1* and K_P=*1.5*, are the sizes of the nMOS and pMOS transistors of the 1x-inverter driver, respectively.

5.3 Avoiding concurrent *ON* state of TSVBOX switches

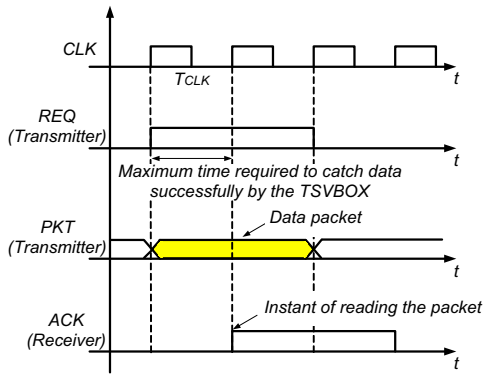

Figure 6: Synchronous handshaking protocol.

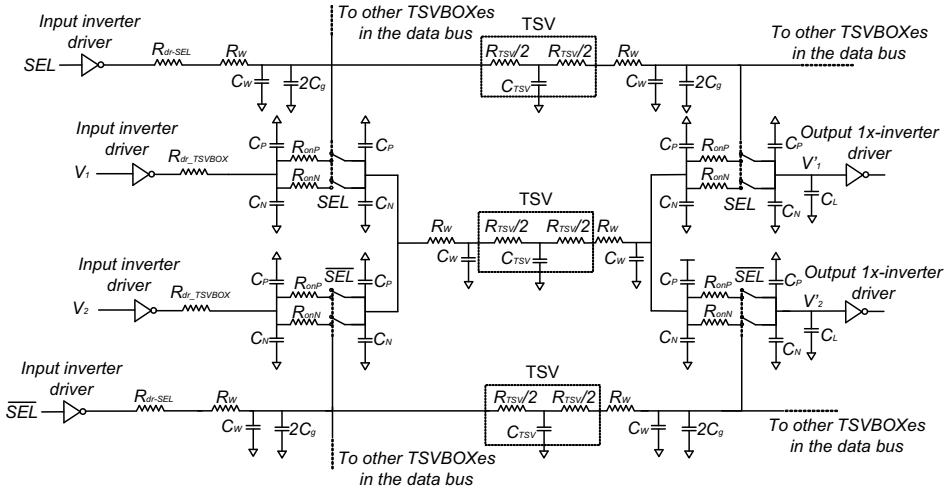

Figure 5: TSVBOX-based 3D NoC 3D path circuit model.

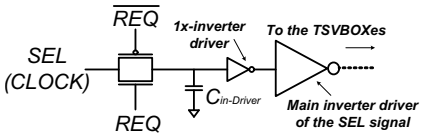

Figure 7: SEL path circuit model after introducing power gating.

As shown in Fig. 8a. At t=$0.5T_{CLK}$, SEL and $\overline{SEL}$ will start discharging and charging, respectively. However, $\overline{SEL}$ will reach the *ON* threshold max(V_{thN}, $|V_{thP}|$) at T_1, while SEL will reach the *OFF* threshold min(V_{thnN}, $|V_{thP}|$) at t=T_2. This because the $\overline{SEL}$ was '0' and SEL was V_{DD}, and '0' is much closer to max(V_{thN}, $|V_{thP}|$), than V_{DD} to min(V_{thnN}, $|V_{thP}|$). It is observable that, during $T_1 \leq t \leq T_2$, all the transmission gate switches of the TSVBOX are *ON* which violates the theoretical behavior of the TSVBOX. To avoid that problem the SEL should discharge fast enough, to reach min(V_{thnN}, $|V_{thP}|$) at t=T_1, as shown in Fig. 8b. This means that the driver resistance of the SEL signal should be smaller than driver resistance of $\overline{SEL}$.

5.4 Minimum clock period for TSVBOX

As shown in Fig. 8, the period of time between $0.5T_{CLK} \leq t \leq T_{CLK}$, can be divided into two smaller periods: $T_{d-\overline{SEL}}$, and the remaining time till the clock edge T_{rem}. During T_{rem}, $V_2{}'$ signal is required to reach an acceptable level '0' or '1', therefore we must select $T_{rem} \geq T_{d-TSVBOX}$. Based on these observations the minimum clock signal for the TSVBOX can be expressed as follows:

$$T_{CLK-min} = 2(T_{d-\overline{SEL}} + T_{d-TSVBOX}) \quad (7)$$

5.5 Different design flows for 3D interconnect

Fig. 9 introduces the design flows for 3D interconnect in case of conventional and TSVBOX-based 3D NoCs. As shown, the first step in both design flows is calculating technology dependent constants and parameters, i.e. RC parasitics, threshold voltages, etc. All other steps in both design flows are concerned with the design of the drivers. The driver resistance can be considered the average value of R_{onP} and R_{onN};

$$R_{dr} = \frac{\frac{R_{onP}}{K_P} + \frac{R_{onN}}{K_N}}{2} \quad (8)$$

where ($K_P \geq 1$, $K_N \geq 1$) are the sizing factors of the pMOS and nMOS transistors, respectively. For all drivers, we choose K_P=$1.5K_N$ to achieve equal currents during charging and discharging. Consequently, Eq. 8 can be rewritten as:

$$R_{dr} = \frac{\frac{R_{onP}}{1.5} + R_{onN}}{2K_N} \quad (9)$$

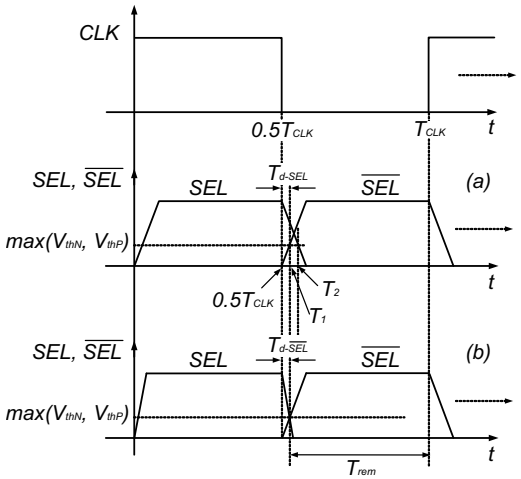

Figure 8: Minimum clock duration for TSVBOX-based 3D NoC, based on the relations between SEL, $\overline{SEL}$, and clock signals.

For conventional 3D NoC, first T_{d-Conv} is to be selected such that; $T_{d-Conv} \leq T_{CLK}$. Then $R_{dr-Conv}$ is calculated using Eq. 3. However, since the driver has minimum size (minimum width and length for each transistor), therefore if the calculated value of the $R_{dr-Conv}$ was larger than the maximum driver resistance (when the size is minimum), $R_{dr-Conv}$ must be set to the maximum allowed driver resistance R_{dr-max}. After that, and based on $R_{dr-Conv}$ value, K_{N-Conv} can be determined from Eq. 9.

In a straightforward way, similar steps can be followed for the TSVBOX to calculate its delays and the corresponding driver sizes.

5.6 Mitigating delay degradation

As noticed from Eq. 4, the conventional 3D NoC outperforms TSVBOX-based one. What makes situation worse, is that data transfer through the TSVBOX is done serially (V_1 during T_H, then V_2 during T_L). Using GALS (Globaly Asynchronous Locally Synchronous) concept, this performance degradation can be mitigated if the vertical communication through the 3D interconnect is done with different clock frequency than other modules of the 3D NoC. According to [9], all the communications between routers is synchronous, the modules running with different clocks can communicate correctly with each other using *REQ* and *ACK* signals. Since TSVs usually shorter in length than other interconnects, then the critical path delay (CP) is always expected to be larger than the TSV delay. As shown in Fig. 10, we assume that the input and

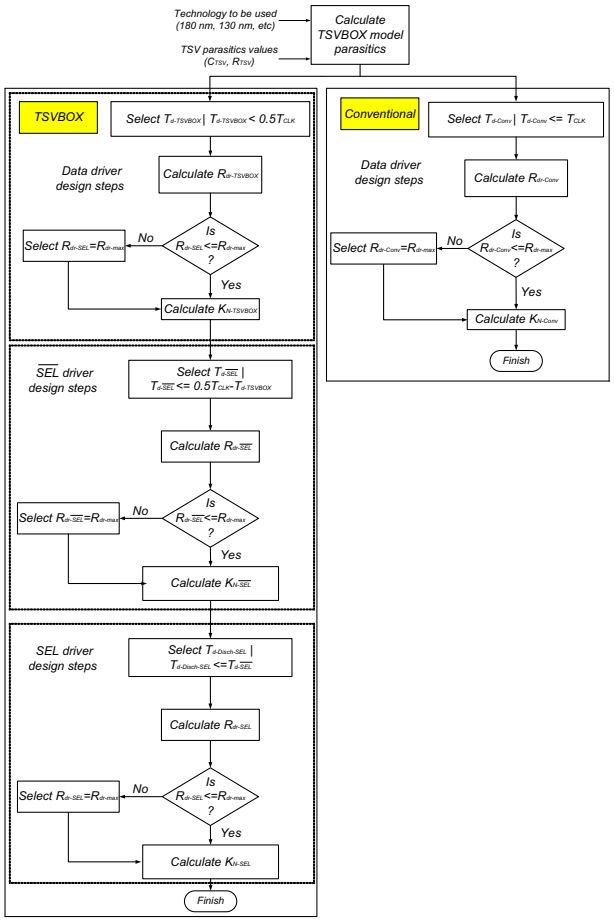

Figure 9: Design flows for 3D interconnect of TSVBOX-based (left) and conventional 3D NoCs (right).

output controllers of the 3D interconnect are running with different clock cycle (T_{CLK-3D}), while all other router modules are running with T_{CLK}=CP. The T_{CLK-3D} is equal to T_{d-Conv}, and $2(T_{d-SEL} + T_{d-TSVBOX})$ for conventional and TSVBOX-based 3D NoCs, respectively.

6. SIMULATION RESULTS

6.1 3D signal path delays

Two frequencies are selected that meet the requirements introduced in Subsection 5.6. Therefore T_{CLK-3D} is selected to be 2.5 and 9.3 nsec, for conventional and TSVBOX-based 3D NoCs, respectively. These values enable us to choose the data drivers with minimum size making the changes only in SEL ($\overline{SEL}$) signal driver, which simplifies the design process. Other router modules run at

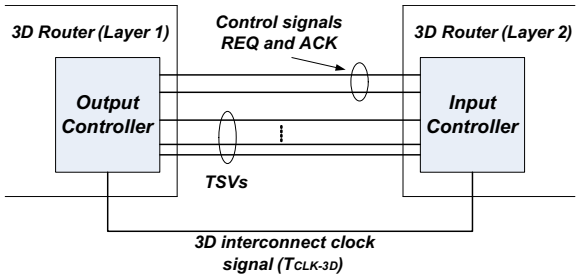

Figure 10: The output and input controllers of the 3D interconnect running at T_{CLK-3D}.

Table 2: Theoretical and experimental 3D signals' delays for conventional and TSVBOX paths.

3D signal delay	Unit	Theoretical	simulation	$\|error\|$
T_{d-Conv}	nsec	2.499	2.45	0.04%
$T_{d-TSVBOX}$	nsec	4.1455	4.15	0.1%
$T_{d-\overline{SEL}}$	nsec	0.5	0.5	0.0%
T_{d-SEL}	nsec	0.1383	0.12	13.23%

Table 3: Driver sizes and their equivalent *ON* resistances.

Design parameter	Unit	Values
(K_{N-Conv}, K_{P-Conv})	-	(1, 1.5)
$(K_{N-TSVBOX}, K_{P-TSVBOX})$	-	(1, 1.5)
$(K_{N-\overline{SEL}}, K_{P-\overline{SEL}})$	-	(2.7526, 4.1289)
(K_{N-SEL}, K_{P-SEL})	-	(9.9531, 14.93)
$R_{dr-Conv}$	kΩ	15.51
$R_{dr-TSVBOX}$	kΩ	15.51
$R_{dr-\overline{SEL}}$	kΩ	5.6344
R_{dr-SEL}	kΩ	1.5582

T_{CLK}=CP, where CP is hypothetically assumed as a parameter taking the values: T_{d-Conv}, $3T_{d-Conv}$, and $5T_{d-Conv}$ (2.5, 7.5, and 12.5 nsec, respectively). Based on T_{CLK-3D}; all conventional and TSVBOX delays and their associated driver sizes are selected and determined according to the design flows presented in Subsection 5.5 and depicted in Tables 2 and 3. As shown, the error between the theoretical and the simulation delays does not exceed 14%, which indicates the acceptable accuracy of Elmore-delay model. Also, it is observable that both $T_{d-PG-SEL}$ and $T_{d-PG-\overline{SEL}}$ are found to be negligible (0.075 and 0.06302 nsec, respectively), and do not affect our proposed design methodology.

6.2 Performance comparison

In order to test the performance under different scenarios, two traffic patterns are selected to work with; Matrix Transpose (MT) and HotSpot (HS). In MT each node located at (X,Y,Z) sends all its traffic to the node located at (S_X-1-X, S_Y-1-Y, S_Z-1-Z), where (S_X=3, S_Y=3, S_Z=2) is the 3D NoC size. In HS, we assume there is a hotspot node in each layer, to which 50% of the total packets injected in that layer are destined. Therefore the two hotspots would consume on average 50% of the total traffic of the 3D NoC. The packet injection process of each traffic flow is a Poisson random process where the time interval between successive injections is represented as exponential random variable [10]. Poisson distributed injection rate is adopted because it is successfully characterizing performance of multiprocessor applications [11].

Two performance metrics are studied; average delay and throughput. The average delay of a packet is defined as total cycles taken by the packet to cross the network towards its destination node. That delay spans from creation of the packet, to when it is ejected at the destination, including source buffer queuing time. For the average throughput, it is defined as the average ejection rate of the packets at their destination nodes. The simulation warm-up period is set to 1000 cycles in which we avoid calculating results until the network get congested [12]. The simulation runs with 3600 packets; 200 packets are injected by each node, and continued at the prescribed packet injection rate till these packets have all been received, and their average delay and throughput are calculated. It is clear that under MT traffic 100% of the injected packets are crossing the 3D interconnect while this percentage reduces to ≈ 25% in HS case.

The simulation results listed in Fig. 11 shows the performance comparison of the two implemented 3D NoCs; the TSVBOX-based and

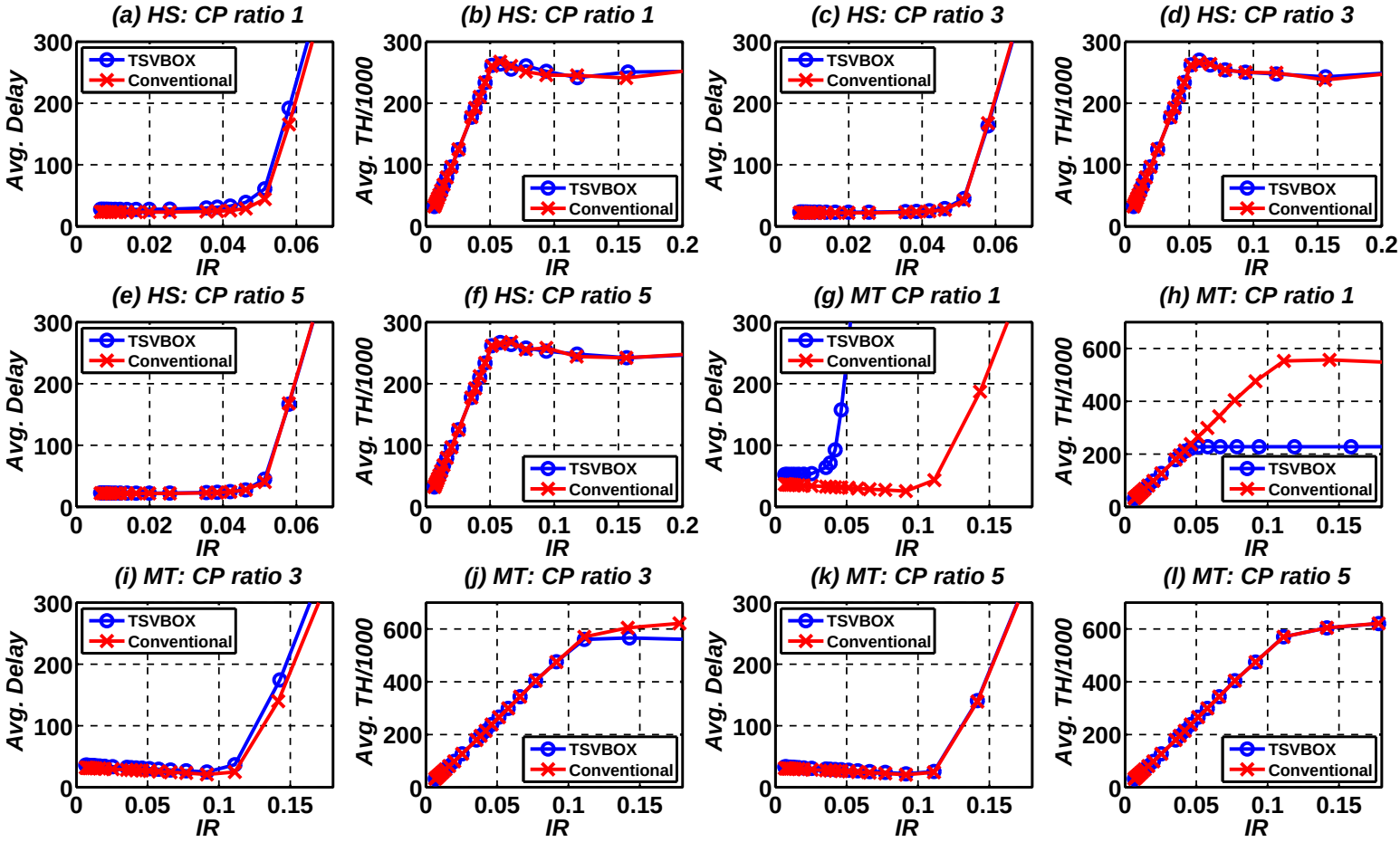

Figure 11: performance comparison between TSVBOX-based and conventional 3D NoCs under HotSpot (HS) and Matrix Transpose (MT) traffic patterns.

convectional ones. As shown, the performance degradation in HS is less than the degradation of MT, because lower number of packets are traversing the 3D interconnect in HS case. hence lower number of packets in HS case will suffer from the TSVBOX delay degradation. Also, for both traffics, as the CP to the conventional 3D interconnect delay ratio becomes larger, the TSVBOX-based 3D NoC shows very close performance to conventional 3D NoC. Because larger CP would mask the delay degradation of the TSVBOX, and reduce its delay effect on the overall performance.

7. CONCLUSIONS

In this paper, the design methodology of the TSVBOX-based 3D NoC is presented in details. Using the proposed methodology, a $3\times3\times2$ mesh topology 3D NoC is implemented using SystemC-A to verify various aspects of the target design. Then, various simulations were conducted to compare the conventional and TSVBOX-based 3D NoCs in terms of delay and throughput. The TSVBOX shows almost no performance degradation versus conventional 3D NoC, especially if the main clock period is larger than the conventional 3D interconnect delay, and also when less number of packets traverse between 3D stack layers as shown in HotSpot traffic case.

8. REFERENCES

[1] M. Said, F. Mehdipour, and M. El-Sayed, *Improving Performance and Fabrication Metrics of Three-Dimensional ICs by Multiplexing Through-Silicon Vias*, 16th Euromicro Conference on Digital System Design (DSD), pp. 581-586, 2013.

[2] I. Loi, S. Mitra, T. Lee, S. Fujita, L. Benini, *A low-overhead Fault Tolerance Scheme for TSV-based 3D Network on Chip Links*, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), pp. 598-602, 2008.

[3] N. Weste, D. Harris, *CMOS VLSI Design, A Circuits and Systems Perspective*, 4th ed., Addison-Wesley, 2011.

[4] A. Papanikolaou, D. Soudris, and R. Radojcic, *Three Dimensional System Integration*, Springer, 2011.

[5] J. Rabaey, A. Chandrakasan, B. Nikolic, *Digital Integrated Circuits, A Design Perspective*, 2nd ed., Prentice Hall , 2003.

[6] R. Jagtap, *A Methodology for Early Exploration of TSV Interconnects in 3D Stacked ICs*, Master thesis, TU Delft, 2011.

[7] *http://www.itrs.net/reports.html*

[8] J. Uyemura, *CMOS Logic Circuit Design*, Kluwer Academic, 1999.

[9] M. Said, A. Shalaby, M. El-Sayed, and V. Goulart, *Flexible router architecture for network-on-chip*, Elsevier Journal of Computers & Mathematics with Applications, Vol. 64, pp. 1301-1310, 2012.

[10] K. Chandrasekar, *Performance Validation of Networks on Chip*, Master thesis, TU Delft, 2009.

[11] D.R. Avresky, V. Shubranov, R. Horst, and P. Mehra, *Performance Evaluation of the ServerNetR SAN under Self-Similar Traffic*, 13th International and 10th Symposium on Parallel and Distributed Processing, pp. 143-147, 1999.

[12] H. Wang, X. Zhu, L.-S. Peh and S. Malik, *Orion: A Power-Performance Simulator for Interconnection Networks*, Proc. MICRO, 2002, pp. 294-395.